REMARKS

Initially, in the Office Action dated October 7, 2003, the Examiner rejects claims 34-53 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,271,110 (Yamaguchi et al.) or U.S. Patent No. 5,592,736 (Akram et al.) or JP patent No. 08 191072 (Takahiro et al.) in view of JP Patent No. 05-121409 (Akira), U.S. Patent No. 5,643,831 (Ochiai et al.) and JP Patent No. 05-206221 (Michihiko et al.).

By this Amendment, claim 34 is amended to correct a minor typographical error. Claims 34-53 remain pending in this application.

35 U.S.C. §103 Rejections

Claims 34-53 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al, Akram et al., Takahiro et al., Ochiai et al and Michihiko et al. Applicants respectfully traverse these rejections.

Applicants have discussed Yamaguchi et al., Akram et al., Takahiro et al., Ochiai et al. and Michihiko et al. in Applicants' previously-filed response and respectfully reassert all arguments submitted in that previously-filed response. The Examiner has now added the Akira reference to the combination of references, asserting that this combination renders the claims of the present application unpatentable.

Akira discloses to increase attaching strength of a bump electrode which is bumped and fixed to the flip chip for an integrated circuit device even if the bump electrode is miniaturized. A v-shaped recess is provided in a semiconductor area of

a chip, and the semiconductor area, including the surface is covered with an insulating film. On top of that, a wiring film of an integrated circuit is laid out. Then, a window is provided on a protecting film covering a chip surface so as to expose the recess and the wiring film. The window part is coated with a thin metal base film connected with the wiring film. On top of that, a projecting metal for a bump electrode is bumped and fixed by electroplating.

Regarding claims 34 and 53, Applicants submit that none of the references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of each of these claims of, inter alia, forming a plurality of pyramidal bump electrodes that includes forming etched holes by anisotropically etching a base material having a crystal orientation, filling up the etched holes by plating a metal, forming a first pattern having openings at positions corresponding to etched holes by etching a first oxidized film formed on a surface of a base material having a crystal orientation, or filling up the etched holes by plating a metal film on a plated feeding film. The Examiner asserts that Akira teaches filling the opening with a copper or gold by electroless plating at 20/26 and paragraph 21. However, Akira discloses the v-type recess being filled with the metal, however, in Akira, the recess is disposed in the semiconductor chip. In contrast, the claims of the present application relate to an etched hole being formed in the crystalline substrate. The crystalline substrate, as recited in the claims of the present application, is not a semiconductor device as disclosed in Akira. Moreover, Akira discloses the recess being disposed for increasing the adherence between the semiconductor chip and

the bump electrode. In contrast, the present application and claims are related to using the figure by separating the bump electrode filled in the recess. Akira does not disclose or suggest these features of the present application.

The limitations in the claims of the present application relate to forming the bumps that includes forming the etched hole by etching anisotropically the crystalline substrate, and filling the etched hole by plating the metal to connect the bump electrode and the pad electrode of the semiconductor device. Akira does not disclose or suggest that a bump electrode is formed separately from the semiconductor device to be connected with the pad electrode later, as recited in the claims of the present application.

Further, Applicants submit that there would be no motivation for one skilled in the relevant art to combine these references in an attempt to achieve the claimed invention, since this combination fails to achieve the limitations in the claims of the present application. For example, Akira discloses that the semiconductor chip disposed in the recess is connected with the bump electrode to increase the mutual adherence. In contrast, Takahiro et al. discloses that the filled conductive resin is utilized by separating the filled conductive resin from the protrusion forming plate disposed in the recess. Therefore, the ideas and features disclosed in Akira are opposite to that disclosed in Takahiro et al. Accordingly, one skilled in the relevant art would have no motivation to combine these references.

Regarding claims 35-52, Applicants submit that these claims are dependent on independent claim 34 and, therefore, are patentable at least for the same reasons noted regarding these independent claims.

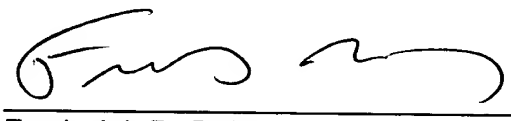
Accordingly, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of each of claims 34-53 of the present application. Applicants respectfully request that these rejections be withdrawn and that these claims be allowed.

In view of the foregoing amendments and remarks, Applicants submit that claims 34-53 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (referencing attorney docket no. 500.38090X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



Frederick D. Bailey
Registration No. 42,282

FDB/sdb
(703) 312-6600